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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/652,044	08/31/2000	Toshimitsu Taniguchi	10417-039001	2951

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EXAMINER
GEBREMARIAM, SAMUEL A

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/652,044	TANIGUCHI ET AL.	
	Examiner	Art Unit	
	Samuel A Gebremariam	2811	

-- Th MAILING DATE of this communication appears on the cov r sheet with th correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *6-28* is/are rejected.

7)☒ Claim(s) *27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of group I, claims 6-21 drawn to a method of making semiconductor device in Paper No. 4 is acknowledged.

Specification

2. Claim 27 is objected to because of the following informalities: 2nd paragraph second line part of the sentence reads "layer continuing". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 6, is rejected under 35 U.S.C. 102(b) as being anticipated by Hsing et al., US patent No. 5,517,046.

Regarding claim 6, Hsing teaches a method of manufacturing a semiconductor device provided with high concentration source/drain layers 32 and 34 respectively of the reverse conductive type formed in a semiconductor layer 20 of one conductive type, a gate electrode 26 formed on a channel layer located between the source and drain layers, a body layer 29 of one conductive type formed in the vicinity of the source layer and a low concentration drain layer 31 of the reverse conductive type formed between the channel layer and the drain layer, wherein the step of forming a body layer of one

conductive type comprises a step of doping impurities of one conductive type into the semiconductor layer by ion implantation (fig. 3 and column 3, lines 7-62).

Regarding claims 7 and 16, Hsing teaches the entire claimed process of claim 6 above including the above process comprising the steps of doping impurities of the reverse conductive type into the semiconductor layer to forma low concentration drain layer 31 of the reverse conductive type; doping impurities of the reverse conductive type into the semiconductor layer to form a high concentration source layer 32 of the reverse conductive type so that the source layer is adjacent to one end of the gate electrode 26 and form a high concentration drain layer 34 of the reverse conductive type in a position apart from the other end of the gate electrode; doping impurities of one conductive type into the semiconductor layer to form a body layer 29 of one conductive type extended from under one end of the gate electrode and formed so that the body layer is adjacent to the source layer 32 of the reverse conductive type; and forming a gate electrode 26 on a gate oxide film 24 after the gate oxide film is formed on the semiconductor layer (fig. 3 and column 3, lines 7-62).

Regarding claim 8, Hsing teaches the entire claimed process of claim 7 above including the step of doping an impurity for forming a reverse conduction type layer by ion implantation (fig. 3 and column 3, lines 38-39).

Claims 22 -26, are rejected under 35 U.S.C. 102(b) as being anticipated by Pfiester et al., US patent No. 4,948,745.

Regarding claim 22, Pfiester teaches a method of manufacturing a semiconductor device comprising source/drain regions 65 and 66 of a second

conductive type in a semiconductor of a first conductive type 54 and a semiconductor layer of a first conductive type constituting a channel 76 located between the source/drain regions of the second conductive type, the method comprising: doping impurities of the first conductive type into the semiconductor of the first conductive type by ion implantation to form the semiconductor layer of the first conductive type (fig. 7).

Regarding claim 23, Pfiester teaches 23 a method of manufacturing a semiconductor device comprising low concentration source/drain regions 63 and 64 of a second conductive type in a semiconductor of a first conductive type 54, high concentration source/drain regions 65 and 66 of the second conductive type in the low concentration source/drain regions and a semiconductor layer of the first conductive type constituting a channel 76 located between the source/drain regions of the second conductive type, the method comprising: doping impurities of the first conductive type into the semiconductor of the first conductive type by ion implantation to form the semiconductor layer of the first conductive type (fig. 7).

Regarding claim 24, Pfiester teaches the entire claimed process of claim 23 above including doping impurities of a second conductive type into a semiconductor of a first conductive type to form low concentration source/drain regions of the second conductive type; doping impurities of the second conductive type into the surface of the semiconductor layer of the first conductive type to form a second conductive type layer; and forming a gate electrode 70 on a gate oxide film 62 provided on the semiconductor of the first conductive type (fig. 7).

Regarding claims 25 and 26, Pfiester teaches the entire claimed process of claim 24 above including the low concentration source/drain regions of the second conductive type are formed to be adjacent to the semiconductor layer of the first conductive type formed below the gate electrode by ion implantation (fig. 7).

Claim Rejections - 35 USC § 103

4 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 9, is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsing in view of Chen et al. US patent No. 5,926,712.

Regarding claim 9, Hsing teaches substantially the entire claimed process of claim 7 above except explicitly stating that the low concentration drain layer of the reverse conductive type or the low concentration source/drain layers of the reverse conductive type are formed so that they are shallow under said gate electrode and they are deep under the high concentration drain layer of the reverse conductive type or the high concentration source/drain layers of the reverse conductive type.

It is conventional and also taught by Chen forming a low concentration drain layer 216 that is shallow under the gate and deeper under the high concentration drain region as claimed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made incorporate the low concentration drain layer taught by Chen in the method of Hsing.

Claims 10-15, 17, 18, 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Hsing.

Regarding claims 10 and 17, Chen teaches a method of manufacturing a semiconductor device, comprising the steps: of doping impurities of the reverse conductive type into a semiconductor layer of one conductive type to form low concentration source/drain layers 216 of the reverse conductive type; doping impurities of the reverse conductive type into the semiconductor layer and forming a layer of the reverse conductive type which ranges to the source/drain layers of the reverse conductive type and is shallower than the source/drain layers of the reverse conductive type; doping impurities of the reverse conductive type into the source/drain layers of the reverse conductive type to form high concentration source/drain layers 219 of the reverse conductive type; and forming a gate electrode 215 on a gate oxide film so that the gate electrode covers said body layer of one conductive type after the gate oxide film 214 is formed on the substrate.

Chen does not teach doping impurities of one conductive type into the layer of the reverse conductive type to form a body layer of one conductive type.

It is conventional and also taught by Hsing to form a body layer 29 by doping impurities of one conductive type as claimed using ion implantation.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the body layer taught by Hsing in the method of Chen in order to improve breakdown voltage.

Regarding claims 11-15, 18 and 19, the combined teaching of Chen and Hsing teaches substantially the entire claimed process of claim 10 above including doping an impurity for forming a reverse conduction type layer by ion implantation after forming the body layer, forming a first gate electrode for a first MOS transistor on a gate oxide film after the gate oxide film is formed on the substrate and forming a second gate electrode 26 for a second MOS transistor on the body layer 29 of one conductive type; and forming source/drain layers of the reverse conductive type so that they are adjacent to the first gate electrode using a resist film coating an area except are as where source/drain layers for the first MOS transistor are formed as a mask (Chen, fig. 2 column 3, lines 35-67 and column 4, lines 1-31 and Hsing, fig. 3 and column 3, lines 38-39).

The limitation using a resist film coating an area is not taught by the combined teaching of Chen and Hsing.

The use of photolithographic process is a well-known process that is commonly used in the fabrication of semiconductor devices.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use conventional photolithographic technique for precise patterning of layers.

Regarding claim 20 and 21, the combined teaching of Chen and Hsing teaches substantially the entire claimed process of claims 12 and 14 above the first MOS transistor is a micro MOS transistor; and the second MOS transistor is a MOS transistor having high resistance to voltage.

The limitation that the above transistor is a micro MOS is conventional device that is commonly fabricated in semiconductor fabrication.

With regards to the limitation that the MOS transistor have a high resistance to voltage, this characteristic is considered to be inherent characteristic of most transistors since any layer have a resistance to voltage value.

Regarding claims 27 and 28, Pfiester teaches substantially the entire claimed process of claim 24 above except explicitly stating using a resist film, as a mask, having an opening in a region for forming the second transistor to form a low concentration second conductive type layer connecting the second low concentration source/drain regions; and doping impurities of the first conductive type by using a resist film, as a mask.

The use of photolithographic process is a well-known process that is commonly used in the fabrication of semiconductor devices.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use conventional photolithographic technique for precise patterning of the layers.

The limitation the semiconductor device comprising a first transistor having high resistance to voltage and a second transistor having high resistance to voltage is not taught Pfiester explicitly.

The claimed characteristic is considered to be inherent characteristic of most transistors since any layer have a resistance to voltage value. Therefore layers 76 and 92 have inherent resistance to voltage value.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References D-G are cited as being related to a method of making semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Samuel Admassu Gebremariam
June 3, 2002

Tom Thomas

TOM THOMAS
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